Application Report

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Center-Aligned SVPWM Realization for 3- Phase 3- Level Inverter

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ABSTRACT

The space vector pulse width modulation (SVPWM) has been widely used in 3- phase inverter control system. The most effective way for the MCU implementation of the SVPWM is the center-aligned PWM, because the PWM module in the MCU can generate the center-aligned PWM easily. This paper discusses the SVPWM implementation, and presents a way to easily implement the center-aligned SVPWM, which can be fit for the on-chip PWM module.

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1 Introduction

The SVPWM has been widely used in 3- phase inverter control system because; it has a higher utility efficiency of DC-side voltage than the sine pulse width modulation (SPWM). Although the SVPWM has many advantages, it is difficult to implement. The most difficult factor is calculating the duty cycles for each power switch, as well as determining the vector sector and pulse sequence in each switching cycle. The duty cycle calculation for the 3- phase 2- level inverter was presented in many papers, and the vector sequence can be determined in many ways (for example, the center-aligned method, which can be easily implemented in MCU platform).

To improve the system efficiency of the 3-phase inverter, the 3-level or multilevel inverter is becoming more popular. Compared to the 2-level inverter, the 3-level inverter has more power switches (up to 12); this means the 3-level inverter has many more vector sectors than the 2-level inverter. So the duty cycle calculation and the vector determination are more complicated in the SVPWM of 3-level inverter than the 2-level inverter.

The paper [1] presented a convenient way to determine the vector sector. Two steps are used to do the process, The first step divides the whole vector area into six main sectors. This step is very similar to the sector determination in that of the 2-level inverters. The second step relocates the reference vector into one of these six main sectors, then divides this main sector into six subsectors. Then the calculation method can be used in the 2-level inverters to determine the effective vectors and calculate their dwell times. But the vector sequence in each switching cycle has not been discussed yet, and the duty cycle calculation method is not easy to implement in the MCU application. The paper [2] uses the same method as [1] to determine the sector. The relocated zero vector is taken as the zero vector in the 2-level inverter vector area, then gives out a similar vector sequence with the 2-level inverter. In the realization, the MCU is used to generate the sequence signal, and uses the peripheral logic circuit to implemented the PWM generation for each power switches. A method that is fit for the MCU implementation without the peripheral logic circuit is not presented.

The most effective way for the MCU implementation of the SVPWM is the center-aligned PWM, for the PWM module in the MCU can generate the center-aligned PWM easily. This paper discusses the SVPWM implementation based on the method mentioned in [1] and [2], and, it presents a way to easily implement the center-aligned SVPWM, which can be fit for the on-chip PWM module.

2 The Basic SVPWM Principle of the 3- Phase 3-level Inverter

Figure 1 shows the hardware topology of the neutral point clamped (NPC) 3-phase 3-level inverter.

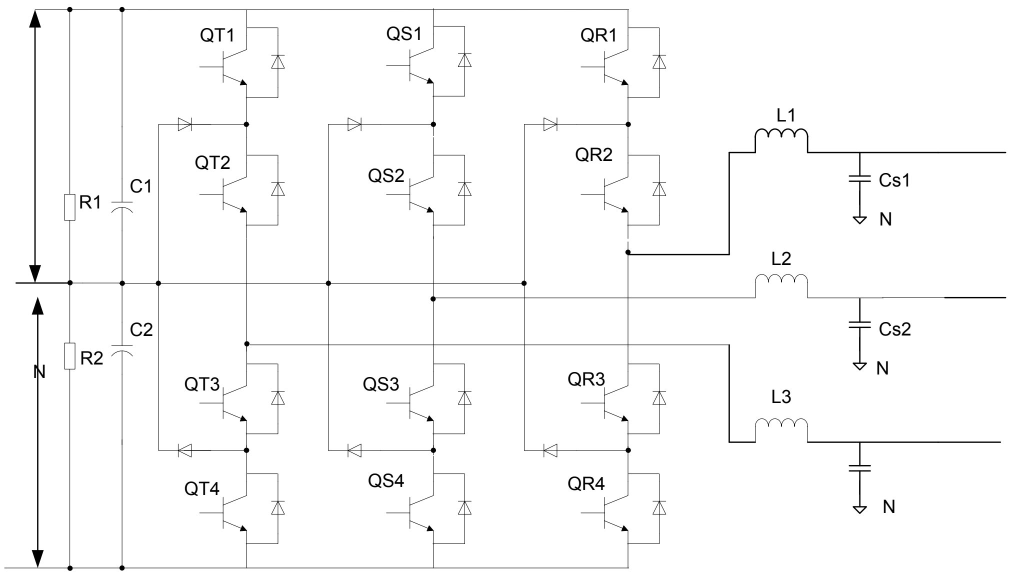

Figure 1. Hardware Topology of NPC 3-Phase 3-Level Inverter

There are three NPC legs (R, S, and T) in the Figure 1; each leg contains four power switches. The four power switches of each leg must be controlled in two complementary pairs. The Qx1,Qx3 (x = R,S,T) is one complementary pair, Qx2,Qx4 is another pair. So, for each leg, it can output three different phase voltage status by controlling the four power switches.

Switch No. / item	Qx1	Qx2	Qx3	Qx4	Phase Voltage	Leg Status
1	ON	ON	OFF	OFF	$\frac{V_{dc}}{2}$	P
2	OFF	OFF	ON	ON	$-\frac{V_{dc}}{2}$	N
3	OFF	ON	ON	OFF	0	O

Table 1. Output Status of Each Leg

There are 27 statuses when controlling the power switches (see Table 1) for each leg; each status can be mapped to the vector diagram of α - β coordinate plane. The 27 vectors can form 18 sectors, as shown in Figure 2.

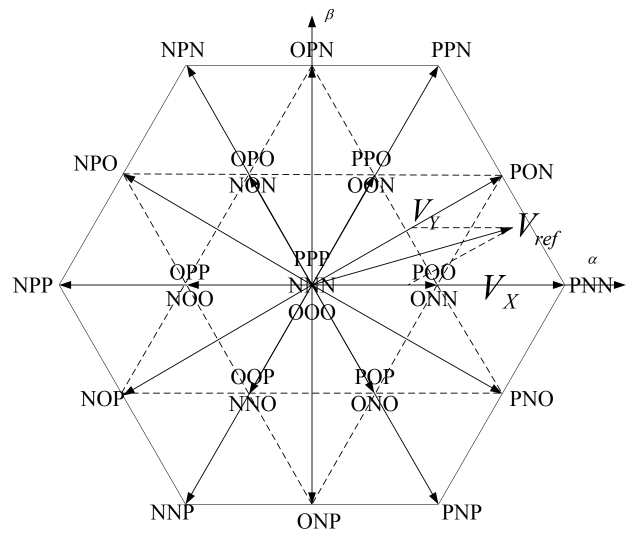

Figure 2. The 3-Phase 3-level Inverter SVPWM Vector Diagram

Assume a reference vector V_{ref}. According to the theory of the SVPWM, we must find out two nearest vectors V_X, V_Y and one zero vector V_Z in Figure 2 to form the vector V_{ref}. Figure 2 shows the relationship between V_{ref} and V_X, V_Y, V_Z. So the vector PNN(V_X), PNN(V_Y), and NNN(V_Z) can be selected to form V_{ref}. If the dwell time of V_X, V_Y, V_Z in a specified interval T_s are T_X, T_Y, T_Z respectively, the following functions must be satisfied:

$$V_X T_X + V_Y T_Y + V_Z T_Z = V_{ref} T_s$$

$$T_X + T_Y + T_Z = T_s$$

However, it is difficult to determine V_X, V_Y, V_Z by the angle only, which is used in the 2-level SVPWM, because the reference vector can be located in different sectors even if the angle is the same. To determine the sector, the amplitude of the reference vector is also needed, but this increases the complexity of the calculation.

[1] and [2] presented a simplified way to determine V_X, V_Y, V_Z. First, the whole vector diagram shown in Figure 2 is divided into six main sectors. Each main sector contains 10 original sectors which can form a subhexagon. The six main sectors distribute continuously with a 60-degree angle difference. Figure 3 shows the six main sectors.

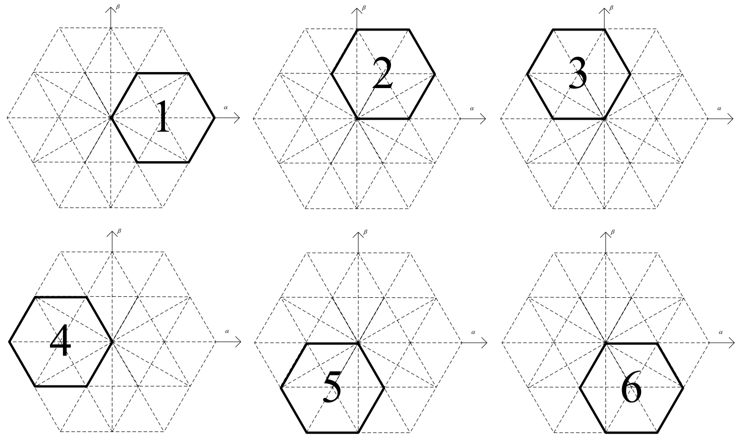

Figure 3. Main Sectors for 3-Level SVPWM

For a given reference vector V_{ref}, the main sector can be determined by using the angle only. For example, in Figure 4, the angle θ between V_{ref} and α axis is between +60 and –60 degrees, which means the main sector of V_{ref} is sector 1.

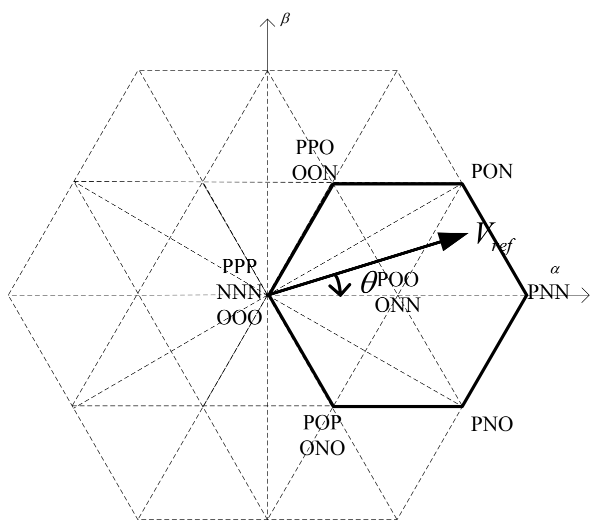

Figure 4. Main Sector 1

After the main sector is determined, it must map the original vectors into the selected main sector. The mapping algorithm follows:

$$V' = V_{original} - V_{map}$$

For example, the original vectors in the main sector 1 are PPP(OOO,NNN),POP(NON),PNO,PNN,PON,PPO(OON),POO(ONN). To get a hexagon similar to the 2-level SVPWM, take POO(ONN) as the mapping vector $V_{map1} = V_0$. After the mapping, we can get the hexagon shown in Figure 5, which is the same vector diagram as the 2-level SVPWM. In this hexagon, there are seven mapped vectors, which form six subsectors in the hexagon.

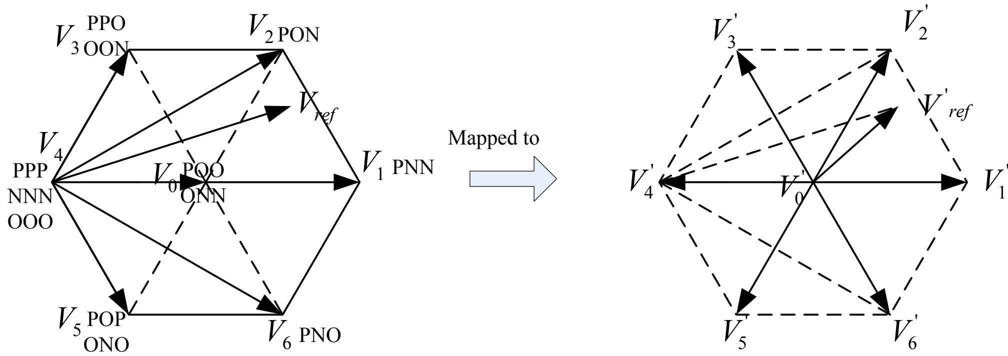

Figure 5. Mapping for Main Sector 1

From Figure 5, we see that V'_{ref} is in subsector 1, and we can easily determine the dwell vector is V'_1 and V'_2. The V'_0 can be taken as the zero vector in the 2-level SVPWM. So, we can get the following function:

$$V_1^{'}T_X + V_2^{'}T_Y + V_0^{'}T_Z = V_{ref}^{'}T_s \quad \textbf{(2)}$$

$$T_X + T_Y + T_Z = T_s \quad \textbf{(3)}$$

Combining equations (2) and (3), produces:

$$(V_1 - V_{map1})T_X + (V_2 - V_{map1})T_Y + (V_0 - V_{map1})T_Z = (V_{ref} - V_{map1})T_s$$

So

$$V_1 T_X + V_2 T_Y + V_0 T_Z = V_{ref} T_s \quad (4)$$

From (4), if the dwell time of V'_1, V'_2, and V'_0 can be calculated, the original vector dwell time can be determined. From the mapping in Figure 5, the vector selection and the dwell time calculation of the 3-level SVPWM are converted to 2-level SVPWM totally.

Different main sectors have different mapping vectors. Table 2 summarizes the mapping vector for each main sector.

Main Sector No.	Mapping Vector	Element of α	Element of β	
1	POO or ONN	$\frac{V_{dc}}{3}$	0	
2	PPO or OON	$\frac{V_{dc}}{6}$	$\frac{\sqrt{3}V_{dc}}{6}$	
3	OPO or NON	$-\frac{V_{dc}}{6}$	$\frac{\sqrt{3}V_{dc}}{6}$	
4	OPP or NOO	$-\frac{V_{dc}}{3}$	0	
5	OOP or NNO	$-\frac{V_{dc}}{6}$	$-\frac{\sqrt{3}V_{dc}}{6}$	
6	POP or ONO	$\frac{V_{dc}}{6}$	$-\frac{\sqrt{3}V_{dc}}{6}$	

Table 2. Mapping Vector for Each Main Sector

3 Simplified Method to Determine the Main Sector

The main sector can be determined by the angle of the V_{ref} in the α - β coordinate plane. As shown in Figure 2 and Figure 3, each main sector is located in the fixed angle range. For example, the angle range of the first main sector is [$-\frac{\pi}{3}$, $\frac{\pi}{3}$]. It is also possible to determine the angle range of the second main sector is [0, $\frac{2\pi}{3}$]. So the overlapped area between the first and second main sectors, can extend to the two adjacent areas. These overlapped areas increase the difficulty of determining the main sector. To specify a monopolized angle area for each sector, we can redefine the main sector as shown in Figure 6.

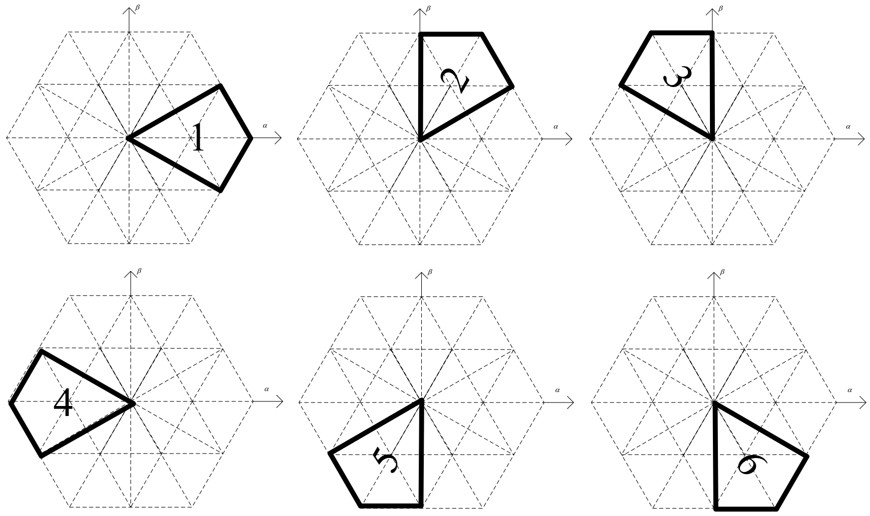

Figure 6. New Definition for the Main Sector

By the definition shown in Figure 6, each main sector has its own angle area and its own subsectors.

Considering the 3-phase voltage waveform shown in Figure 7, the corresponding main sector is labeled in the correct position. From Figure 7, the relationship between the main sector number and the three phase elements can be summarized by Table 3, which can help to determine the main sector easily.

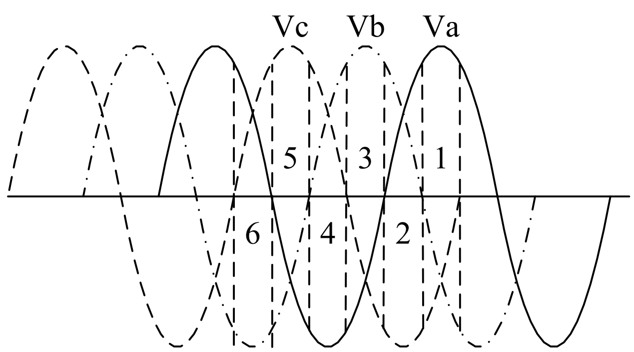

Figure 7. Main Sector Location

Va	Vb	Vc	Main Sector No.
>0	<0	<0	1
>0	>0	<0	2
<0	>0	<0	3
<0	>0	>0	4
<0	<0	>0	5
>0	<0	>0	6

Table 3. Main Sector Determination

4 The Subsector Process

In the 2-level SVPWM, the first step is to find the sector number which can determine the dwell vectors. The second step is to calculate the dwelling time for each selected vector. According to the principle for 3-level SVPWM in Chapter 1, when the main sector is determined and all the vectors are mapped to the main sector, the same process done in 2-level SVPWM can be implemented to determine the subsector and calculate the dwelling time for each dwell vectors. This process algorithm had been discussed in many papers, so this paper will not discuss the sub-sector determination and the dwelling time calculation.

Although we can find the dwelling time for each vector by the subsector process, the distribution of the duty cycles for each power switch is much more complicated than the 2-level SVPWM. The 3-level SVPWM has six pairs of complementary power switches, which means when we get the dwelling time of the selected vector, six duty values must be calculated. To simplify the duty cycle calculation, this paper discusses an effective way to calculate the duty cycle for each pair of power switches easily.

We will also take the main sector 1 for example. According to Figure 4, there is no N status for the R phase. Besides, if OON, ONO, and OOO are selected for the vector mapping, there will be no P status for the S and T phases. For the R phase, replace the P status with 1, and the O status with 0. For S and T phases, replace the O status with 1, and the N status with 0. The same vector diagram as the 2-level SVPWM is the result. Figure 8 shows this operation.

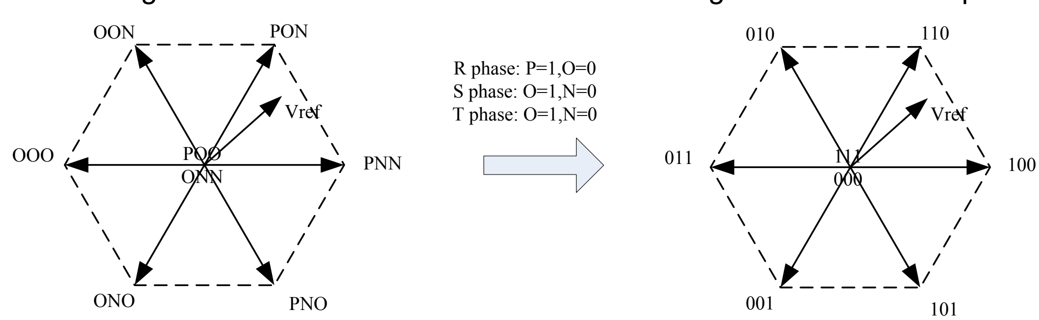

Figure 8. The Status Replacement

After doing the 2-level SVPWM process, the dwelling time for three vectors can be determined. As shown in Figure 8, T_X is the dwelling time of 100, T_Y is the dwelling time of 110, and T_Z is the dwelling time of 111 and 000. So we can calculate the three duty cycles for three pairs of complementary power switches, (d1, d2, and d3) with the center-aligned PWM output mode; the resulting vector sequence for this example is $000 \rightarrow 100 \rightarrow 110 \rightarrow 111 \rightarrow 110 \rightarrow 100 \rightarrow 000$. The left side of Figure 9 shows status of the upper switch of the three pairs of complementary power switches in the 2-level SVPWM, which is called center-aligned SVPWM.

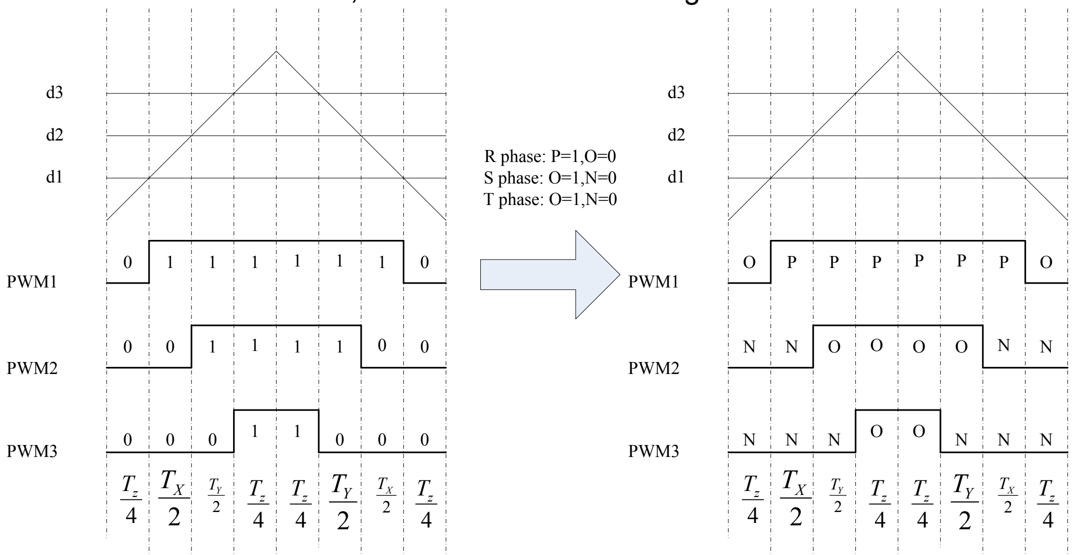

Figure 9. Center-Aligned SVPWM for 2-Level Inverter

If we replace 1 and 0 with P and N, respectively we get the right part of the center-aligned SVPWM for a 3-level inverter. The vector sequence for the 3-level SVPWM is:

$$ONN \rightarrow PNN \rightarrow PON \rightarrow POO \rightarrow PON \rightarrow PNN \rightarrow ONN.$$

The positive pair of power switches is Qx1 and Qx3(x = R,S,T); the negative pair of the power switches is Qx4 and Qx2(x = R,S,T). We also define the same status 0 and 1 for each pair as the 2-level SVPWM. So for the main sector 1, in the single switching cycle, the negative pair of R phase is always 0, for the S,T phase, the positive pair is always 0. Then only three pairs of power switches must be controlled with the different duty cycles, the positive pair of the R phase, and the negative pair of the S,T phase, which are equal to the three pairs power switches in the 2-level SVPWM. That means in the main sector 1, d1 can be assigned to positive pair of R phase, d2 can be assigned to the negative pair of S phase, and d3 can be assigned to the negative pair of T phase.

The result of the preceding analysis can be extended to other vectors. Table 4 summarizes the status replacement and Table 5 shows the duty cycle assignment for each main sector.

Main Sector No	R Phase		S Phase		T Phase	
	0	1	0	1	0	1
1	O	P	N	O	N	O
2	O	P	O	P	N	O
3	N	O	O	P	N	O
4	N	O	O	P	O	P
5	N	O	N	O	O	P
6	O	P	N	O	O	P

Table 4. Status Replacement for Each Main Sector

Main Sector No.	R Phase		S Phase		T Phase	
	Positive	Negative	Positive	Negative	Positive	Negative
1	d1	0	0	d2	0	d3
2	d1	0	d2	0	0	d3
3	0	d1	d2	0	0	d3
4	0	d1	d2	0	d3	0
5	0	d1	0	d2	d3	0
6	d1	0	0	d2	d3	0

Table 5. Duty Cycle Assignment for Each Main Sector

5 The Algorithm Implementation

From the analysis in Section 4, we can implement the 3-level SVPWM algorithm. Figure 10 shows the software flow diagram.

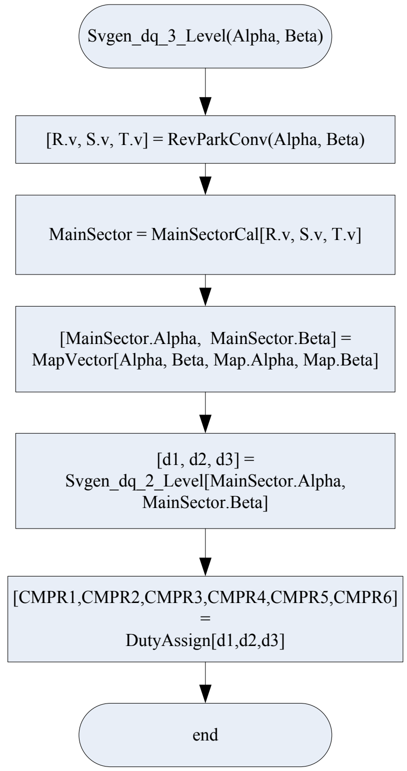

Figure 10. Flow Chart for 3-Level SVPWM Algorithm

In Figure 10, all function inputs are α β elements of the reference vector.

RevParkConv is the function of the reverse conversion of the Park, from which we can get the three phase static elements.

MainSectorCal is the function to determine the main sector number by using the result listed in Table 3.

MapVector is the function to map the reference vector to the selected main sector. The

α β elements of the mapping vector are listed in Table 2.

Svgen_dq_2_Level is the function to implement the 2-level SVPWM process, from which we can determine the three duty cycles d1, d2, and d3.

DutyAssign is the function to assign the CMPR value for each pair of power switches by using the result listed in Table 5.

6 The Simulation Result

To test the validity of the algorithm discussed in Chapter 5, the simulation result is given by using the Matlab Simulink Platform. All the algorithm has been implemented by the C code s-function, which can transplant to the real system easily.

The simulation conditions are:

- Three-phase three-level NPC bridge
- Switching frequency: 10 kHz, PWM period count: 3000
- DC-side voltage: 700 V
- Reference phase-to-phase voltage: (1) 220 V/50 Hz; (2) 280 V/50 Hz
- LC filter parameter: L = 9 mH, C = 4.7 µf for each phase
- R load: 100 Ω for each phase
- Without dead-time

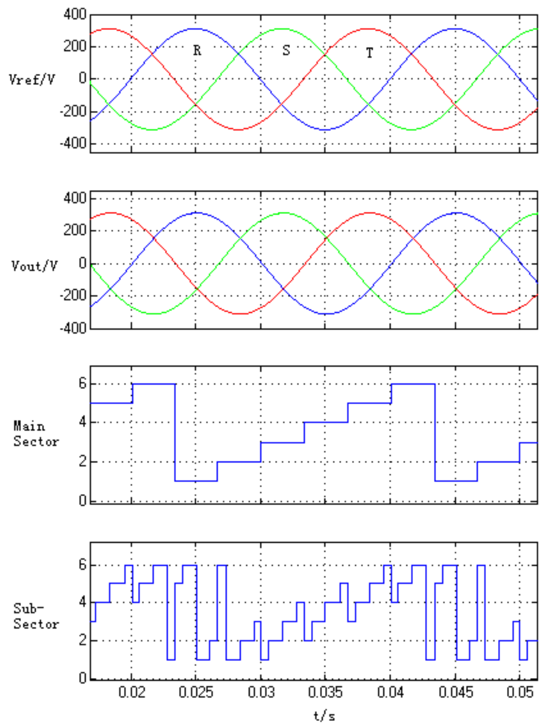

Figure 11. Simulation Result

(CH1: Reference Voltage; CH2: Output Voltage; CH3: Main Sector Calculation; CH4: Subsector Calculation)

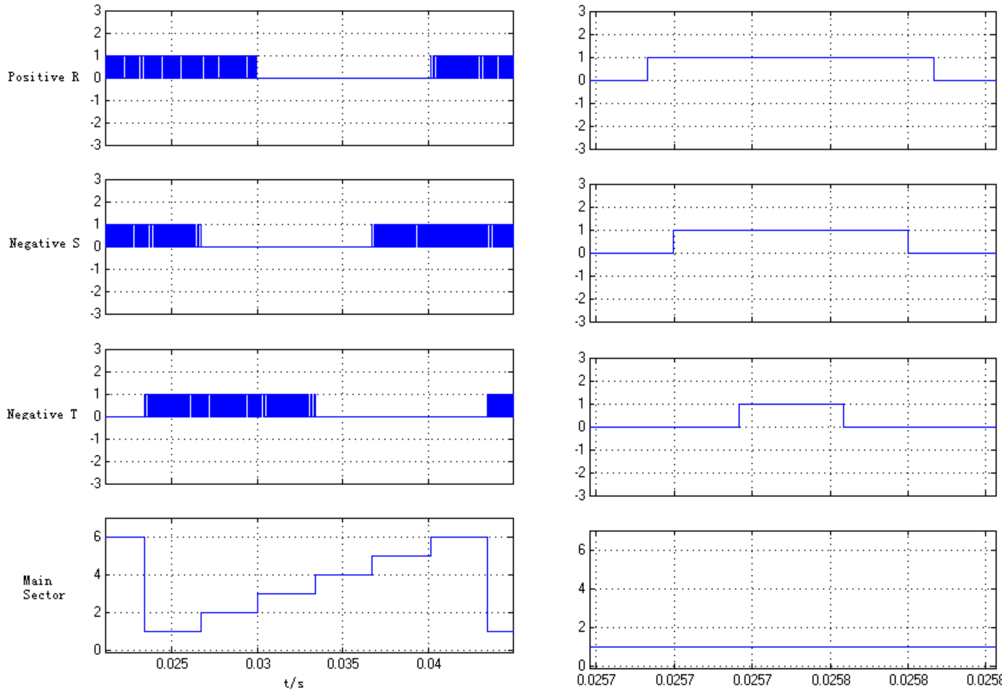

Figure 12. Simulation Result

(CH1: Positive QR1 PWM; CH2:Negative QS2 PWM; CH3: Negative QT2 PWM;

CH4: Main Sector)

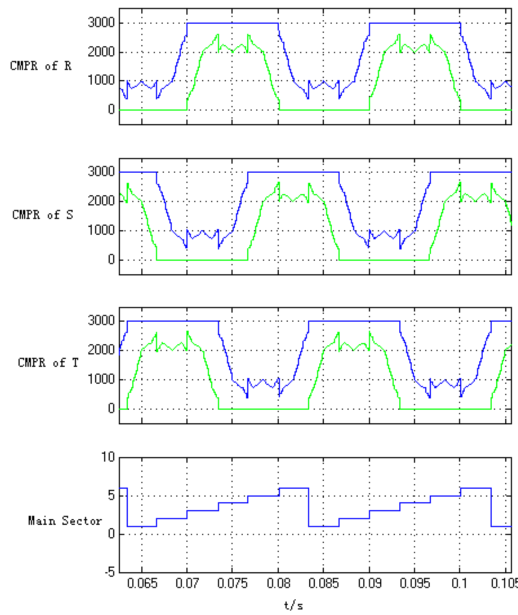

Figure 13. CMPR Value for 220Vac Output

CH1: CMPR Value for R Phase Positive (Blue) and Negative (Green)

CH2: CMPR Value for S Phase Positive (Blue) and Negative (Green)

CH3: CMPR Value for T Phase Positive (Blue) and Negative (Green)

CH4: Main Sector

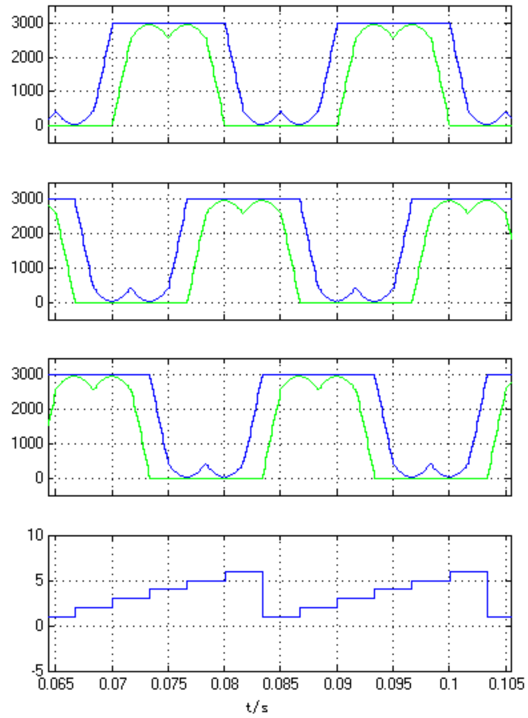

Figure 14. CMPR Value for 280Vac Output

CH1: CMPR Value for R Phase Positive (Blue) and Negative (Green)

CH2: CMPR Value for S Phase Positive (Blue) and Negative (Green)

CH3: CMPR Value for T Phase Positive (Blue) and Negative (Green)

CH4: Main Sector

From the simulation result shown in Figure 11 through Figure 14, the algorithm is proved to be correct. The algorithm can be used to implement the 3-level 3-phase inverter SVPWM. However, because the impact caused by the dead-time and the unbalance of the DC side voltage are not considered, further research is required. Therefore, we must pay special attention to the limitation of the method.

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