Generating High Voltage with High Fidelity at High Power using a Modular Multi-Level Converter (M2LC)

Michael E. Aiello
2/4/16

MEA Consulting
Abstract

The Modular multi-level converter (M2LC) is a fairly new technology. It can be considered the next step in the evolution of the traditional cascaded H-bridge converter by which the cascaded cells do not require a rectified secondary of a transformer to sustain DC voltage.

The traditional M2LC control will not allow low frequency or DC operation of the converter unless special modulation techniques are added to the algorithm¹.

However one of the many benefits of the M2LC is the ability to create a converter operating at an ultra high voltage (UHV) without the use of a transformer which introduces issues of isolation breakdown in the system. This has been done successfully in China with a M2LC sustaining a transmission line that operates in excess of 1 GV DC². The cell stacking nature of the M2LC requires only the that the communication interface be isolated. This is usually done with fiber optics³.

To date, the traditional approach in the design of the M2LC cell structure is to use 1200 or 1700 volt IGBT modules to control the switching of the cell capacitors. The capacitor type is typically a single 1100 volt film. This approach for the construction of the cell has been shown to be the most robust for energy conversion applications⁴.

Given this traditional approach to M2LC design, a question is posed as to the validity of a design that would use lower voltage (600 volt) IGBT's coupled with lower cost electrolytic capacitors (400-450 volt). We know instantly that such a design would require more control electronics. In addition, the use of low cost electrolytic capacitors, which process capacitance values that are much higher then the film capacitor per unit volume, would reduce the current rating of the converter due to degradation effects in the electrolyte.

This paper will show that given these drawbacks, a case can be made for the use an M2LC that comprises these elements. In fact it will be shown that new applications for the M2LC can be realized with a converter constructed with these components.

¹ See http://mea-consulting.org/m2lc-software/
² See https://en.wikipedia.org/wiki/Ultra-high-voltage_electricity_transmission_in_China
³ See http://mea-consulting.org/m2lc-hardware/
⁴ See http://www.engineering.pitt.edu/Sub-Sites/Conferences/EPIC/_Documents/2014-Conference-Documents/PE--Aiello_pdf/
**Background**

A traditional M2LC cell operates as three levels\(^5\). The voltage rating is usually 600-700 volts if 1200 volts IGBT's are used or 1100-1300 volts if 1700 are used. As mentioned in the abstract above, the cell capacitors are usually of film based construction in order to operate reliably at high ripple currents.

This design approach has been shown to be the most economical for applications such as motor control.

For application limited to 200 amps, there is the possibility of including 600 volt IGBT's in a M2LC cell which could operate at between 300 and 400 volts. However, two factors limit the viability of this choice. First, film capacitors at this voltage are very expensive and would be considered *special order* components. The alternative is the so called computer grade electrolytic capacitor which cannot stand up to the ripple current commands demanded by typical applications such as motor control.

However, if one were to identify new and special applications for the M2LC that would require a high quality factor for voltage and current control and be able to be modulated at high frequency, then certainly a case can be made for its construction based on 600 volt IGBT's and electrolytic cell capacitors.

Before embarking on a proposal for a design of an M2LC cell that utilized 600 volt IGBT's and electrolytic capacitors, I direct the reader to the paper *High Performance M2LC System*. This document provides a general background for the design of a high performance M2LC. The proposal presented here can be considered a variant of the design outlined in this paper with exceptions as noted.

**Multi-Level Cell Design**

An outline of an M2LC cell module utilizing 400 volt cells is shown in Figure 1 below. There are six switches that when combined will form a cell module that operates at seven levels. The cell incorporates *cell bypass* (a latching relay crowbar circuit), a distributed inrush soft-start circuit (charging thermistor and bypass relay) and a 15 KV isolation control transformer and power supply. Other then these exceptions, the design of the cell is as outlined in the reference paper cited above.

This cell module is proposed to operate at 50 amps rms. As such the relays and thermistors are PC board mount\(^6\). Bypass and inrush relays are controlled by the low speed LDD/LED POF connection. Control communications is proved by the high speed GOF SFP connections.

Nominally, the cell would be designed to operate at 1800 volts with the IGBT's operating at a very conservative rating of 300 volts. However, the cell would be designed to withstand a sustained operating voltage of 2400 (IGBT's operating at 400 volts) if one or more faulty switches are placed in the *crowbar* state within the cell stack.

A schematic and assemble diagram for this proposed module is shown in Figure 1 and 2 below.

---

\(^5\) Two IGBT half bridge modules are connected together. The minus bus of the top bridge is connected to the plus bus of the bottom bridge. The two exiting connections are tied to each of the half bridge mid-points.

\(^6\) The relay is Alibaba SY7, 50 amps 250 AC. The thermistor is a standard NTC disk type.
Figure 1  Multi-Level Cell module schematic.
Control power circuit

Epoxy Encapsulated Module

Latching relay crowbar circuit

Charging bypass relay

Hall effect transducer

Charging thermistor

High current electrolytic capacitors

Approx. 10.0" (254 mm)

Approx. 8.6" (218 mm)

Approx. 20.6" (523 mm)

15 KV isolated control transformer and power supply

Figure 2 Multi-Level Cell module assembly.
The dimension shown in Figure 2 are approximate. Note the three IGBT modules and the two sets of electrolytic capacitors associated with each module. The IGBT modules are mounted between the bottom of the PC board and the heatsink. The capacitors are mounted on the top of the PC board with bus bars extended from the board.

The capacitors are positioned in such a way as to allow the unrestricted layout of other PC board components such as opto-isolators, IGBT gate drivers, the gate transformers and of course the FPGA.

As described in the reference paper *High Performance M2LC System* cited above, it is recommend that all PC board control components (most importantly the FPGA and SFP) be encapsulated in epoxy to reduce the chance of a flash-over fault form the power components. The ability to maintain communications to the board in lieu of a catastrophic fault ensures uninterrupted communications to the adjacent cell modules.

To reduce the complexity of the power traces on the PC board a special IGBT module has been selected for this design. It is an Infineon™ F3L75R07W2E3_B11-DS neutral-point clamp module. A diagram of this module with the associated electrolytic capacitors is shown in Figure 3 below.

![Diagram of signal 680 V 3-Level switch.](image_url)

**Figure 3** Diagram of signal 680 V 3-Level switch.

The use of this module requires only four connections to the PC board. With the two sets of capacitors, a three-level switch can be realized. The drawback in using this module is that during operation, either two diodes or two IGBT switch paths are required to complete the circuit. This effectively doubles the DC losses compared to the equivalent three-level switch comprised of two half-bridge IGBT modules. If one looks at the estimated dimensions for this IGBT module as shown in Figure 2 above and Figure 4 below, it appears that there is more than enough room to replace the single IGBT neutral-point clamp module with two traditional *dual* modules if it is found these extra losses are unacceptable.

The sub-assembly diagram for the circuit in Figure 3 is shown in Figure 4 below. Two sets of three electrolytic capacitors of *computer grade* construction, are stacked one on top of the other. Electrolytic *tubular* capacitors come in a wide range of diameters. Here I choose three 1 and 3/8 inch
diameter capacitors connected in parallel rated at 450 volts each with a value of 1200 uF.

The selection of four (plus two optional) 1 and 3/8 (instead of say two 3000 uF 3 inch diameter) capacitors provides for a higher ripple current rating in a smaller footprint.

The selection of the size of these capacitors is also dictated by the current rating of module (50 amps rms). This will be described in more detail below.

**High Voltage Control Transformer**

A single phase of a M2LC is constructed using multiple cell modules outlined in Figure 1 and Figure 2 above. *High Performance M2LC System* mentions some ideas on how to generate the control voltage that power the circuitry and IGBT drivers contained within each of the cell module.

One idea mentioned in this paper is a lithium ion battery start-up circuit and a circuit comprised of a current transformer (CT) that would switch out the battery and sustain the control supply after the converter begins operation\(^7\). This works well only if it can be guaranteed that converter is operating in mode that would sustain enough current flow to sustain the CT power supply. In other words, as converter for controlling a motor that operated with variable load, this approach would not work.

---

\(^7\) There has been discussions relating to deriving the control supply from the DC voltage provided by the cell capacitors. However, this approach relies on the condition that the cell can maintain operation without fault which defeats the idea of an optional cell by-pass circuit. Without the supply, the normal communications channel is broken and cannot extend it's communications to it's peer modules. Only the optional redundant communications loop can maintain one failure in the chain. After that, the entire chain (phase) ceases to operate.
A better solution is a high voltage control transformer that derives its power from a standard 115/230 VAC source. A schematic for one proposed design is shown in Figure 5.

The design uses a Power Integrations™ TopSwitch that can operate with a rectified 115 or 230 VAC supply. The control component used in this design are essentially a template design recommended by Power Integrations application notes except for a bifilar wound primary winding.

The isolated secondary winding\(^8\) must be kept at a distance of at least 5mm away from the ferrite UU core. This winding must also be encapsulated with a voltage epoxy potting compound drawn in a very high vacuum environment.

The 5mm distance from the core creates excessive leakage inductance as viewed from the primary winding. For this reason the primary must be wound bifilar and a clamping diode added to catch the flux caused by the excessive leakage inductance on the secondary winding.

---

\(^8\) The side that connects to the cell module shown in Figure 1.
The entire transformer and power electronics are then potted with standard epoxy to create a ridged structure. This is shown in Figure 6.

![Figure 6](image)

**Figure 6** 15 Kv isolated control transformer dimensions.

The control transformer is then attached to the cell module as shown in Figures 1 and 2 above.

**Forty Nine Level M2LC System**

Using the mult-level cell module described in Figure 1 and 2 above as a build block, a complete M2LC can be created with the addition of only a single control module (CTRL module). The CTRL module is explained in detail in High Performance M2LC System.

An example of one such configuration is shown in Figure 7 below. Here three sets of sixteen multi-level cell modules outlined in Figure 1 and 2 above are connected together to form a three-phase DC/AC\(^9\) converter that can operate from a 15 KVDC bus.

The diagram shown in Figure 7 represents a complete system that can be directly connected to a 15KV DC bus or connected directly to an active 11 KV AC three phase supply creating the 15 KV DC bus. This is because the pre-charge circuits are built into each multi-level cell module\(^{10}\).

These charging circuits (as well as the bypass relay) are controlled by a separate low speed plastic fiber optic connection (LDD/LED) controlled by the CTRL module that is daisy chained between each of the multi-level modules. The high speed SERDES connections (SFP) also contained on the CTRL module are daisy chained between each of the multi-level modules. This is as viewed from Figure 7-c (Front view) below.

---

\(^9\) Or AC/DC since the converter can operate in 4 quadrants.

\(^{10}\) The components labeled charging thermistor and charging bypass relay shown in Figure 1 and 2.
Figure 7  A 49 Level 3-Phase M2LC stack operating from a 15 KV DC Bus
A single LDD/LED daisy chain connect all the multi-level modules of all three phases to the CTRL module. In addition three separate SFP daisy chains, one for each phase are daisy chained between the CTRL module each of the three phase stacks. This is done for reasons of performance.

Note that both the LDD/LED fiber and SFP fibers have a redundant return path back to the CTRL module. This is done in the event that a given multi-level module's communications may fail. Under these conditions, operation can be maintained with IGBT switches contained on the failed multi-level module placed in bypass mode.\(^{11}\)

As viewed form Figure 7-b (Back view), the controlled 11 KV AC connections are made at the mid-point connects of the stacked multi-level modules. These connections labeled Minus Terminal and Plus Terminal in Figures 1 and 2 are also daisy chained on each of the multi-level module stacks that define the three phase connections of the M2LC.

Also as viewed form the back is the 115/230 V AC control power that is bussed to each of the high isolation control transformers described in Figure 5 and 6 above.

**Electrolytic Capacitor Ripple Current**

As mentioned above, for the harsh operating condition of a typical M2LC application, film capacitors are preferred over electrolytic capacitors.

Regardless of this constrain it must still be emphasized that for a given volume the electrolytic capacitor can store much more charge then the film capacitor.

Given this it would be good at this point to get a general idea as to how much ripple current flows through these link capacitors, let say for an output current of 50 amps RMS.\(^{12}\)

Figure 1 of document [M2LC Resonance Mode](#) shows the configuration for the simulation of a 5 level M2LC. This paper addresses a special operating mode that uses circuit resonance to allow the M2LC to operate at very low frequency or at DC.

For now we are only interested in the so called Normal Mode described starting at page 5 of this document.

We configure the simulation to draw 50 amp RMS as a current source (labeled $i_a$ in Figure 1 of document M2LC Resonance Mode) at the load connection labeled $MLvl_vs_a$ lagging the applied voltage by 30 degrees. A plot of this is shown in Figure 8 below.

The level count is 5 with the cell capacitors set at 400 uF. This setup is obviously radically different from the M2LC configuration of 49 levels with an effective capacitor value of 3600 uF proposed in this paper. It is enough however to get an idea of the expected ripple current in the cell capacitors with a 50 amp RMS load rating.

---

\(^{11}\) See Appendix A of [High Performance M2LC System](#).

\(^{12}\) It must be noted here that in the case of the M2LC it does not matter if this current is reactive or real.
Figure 8  Simulation of 5 level M2LC running with a 50 amps RMS load current.

Figure 9 below shows what the expected ripple current of the cell capacitors would be under these conditions. The current labeled $MLvl\_i2$ in Figure 1 of the cited document is the capacitor current. This is plotted with load current $ia$. 
Figure 8  Plot of 50 amps RMS load current with capacitor current.

Processing the signal $MLvl_{i2}$ through Octave (Matlab) determines that the equivalent RMS current flowing through the capacitor is approximantly 18.5 amps (a cap/load current ratio of .37). The 1200 uF electrolytic capacitors shown in Figure 3 and 4 above are each rated conservatively at 7 amps RMS. If we were to use three in parallel, we have more than enough margin to operate this converter at 50 amps RMS output current.

These finding are backed up with the information found in paper High Resonant Frequency M2LC. Here a test with load current of 89 amps RMS. The measure RMS capacitor voltage came to 30 amps (a cap/load current ratio of .33).

What is not obvious is the simulation described in M2LC Resonance Mode and the simulation/measured results of High Resonant Frequency M2LC are done at what is considered in the industry as a low value of M2LC inter-arm inductance$^{13}$. The value of this inductance effects the capacitor ripple current.

It is suggested in paper High Resonant Frequency M2LC (for which I am in agreement) that the typical high values of inter-arm inductance selected for the purpose of minimizing the $2^{nd}$ harmonic current flow in the M2LC bus has no justifiable argument in improving overall M2LC performance when applied to motor control.

$^{13}$ Also referred to as inter-phase inductance.
Application: A ELF/VLF Transmitter

A 49 level M2LC that utilized electrolytic cell capacitors for use in general power conversion and control applications can not be considered viable for reasons of cost, complexity and reliability.

However, I believe there is one application for this converter design which deserves some degree of exploration. That is as a radio transmitting amplifier for ELF (Extremely Low Frequency) and VLF (Very Low Frequency) communication installation.

Here a single stack of mult-level modules would be used (one phase), the size of the stack determined by the antenna design and the required voltage to create the electromagnetic wave.

There are three aspects that make this design a plausible candidate for this application.

First, we have now justified the use of electrolytic capacitors in a M2LC. Typical ELF operates at 3 Hz and VLF at 2 Khz\(^\text{14}\). At these frequencies, the rate of discharge of cell capacitors would be excessive if not for the use of large electrolytic storage capacitors.

Second, the use of a very high level count for the M2LC allows for very high quality wave generation coupled with the fact that each level can be modulated at 20 Khz rate.

Finally, the high speed communications provided by the SFP SERDES interface allows all multi-level cells to be updated at minimum of 20 KHz. This would allow the converter to operate effectively from 3 Hz up to 2 KHz.

To accomplish this, the control algorithm for the M2LC described in High Performance M2LC System would have to be modified to allow frequency modulation on a selected carrier command signal.

As described in this document, each cell is responsible for generating a carrier reference that when combined with a command, controls the switching state of the given cell. This is done within the FPGA contained in each cell module\(^\text{15}\). All carrier references generated in each cell module are synchronized to the CTRL module\(^\text{16}\).

For normal control of the cells, this synchronization is fixed at 20 Khz (50 uSec). To create frequency modulation however, an additional command needs to be sent to each cell dictating the desired synchronization time to be applied on the next cycle. In other words this command would allow each cell to frequency modulate relative to 20 Khz (e.g., 19.98 KHz, 19.99 KHz, 20 KHz, 20.01 KHz and so forth). This means that the update time is no longer constant but is instead varied with the desired frequency modulation to be applied on the next update cycle.

So now, each command update includes the amplitude modulation command as well as the modulation command that controls the switching period.

\(^{14}\) There is also LF (Low Frequency) communications which is defined for frequencies of 20 to 50 Khz.
\(^{15}\) In the design described in this document, the FPGA of each cell module controls six switches and thus generates six carriers phases. The total number of carriers in the stack is 48, each shifted by 2 PI / 48.
\(^{16}\) With current SERDES technology contained with FPGA's like Xilinx™ Series 7, this synchronization can be done within a view nano-seconds.
For 2 KHz wave generation, the nominal cell switch frequency of 20KHz prides an adequate amount of bandwidth (resolution) for modulation. For 3 Hz, the modulation resolution for all intents and purposes is continuous.